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TITLE: Digital video horizontal synchronization pulse detector and processor

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ABPL:
The invention pertains to a digital video horizontal synchronization pulse detector and processor comprising pulse detector for generating a timing pulse in response to each horizontal synchronization pulse. A sync position error device generates a time position error signal for each timing pulse relative to a corresponding window pulse. A window pulse generator generates the window pulses and limits the time position error signals to a maximum value. An acquisition device tracks when the timing pulses occur inside and outside the corresponding window pulses. An averaging device averages the time position error signals to generate an average error signal. A **counter** phase locks to the timing pulses to generate processed horizontal sync pulses such that when the timing pulses occur within the corresponding window pulses the **counter** is adjusted by the average error signal and when a predetermined number of timing pulses occur outside the corresponding window pulses, the **counter** is loaded with a predetermined value during a timing pulse to align the timing pulses with the corresponding window pulses.

BSPR:
In accordance with the teachings of the present invention, a digital video horizontal synchronization pulse detector and processor for detecting and

processing horizontal synchronization pulses in a video signal is disclosed. The digital video horizontal synchronization pulse detector and processor detects the horizontal synchronization pulses and generates processed horizontal sync pulses to be used to provide horizontal image synchronization, memory mapping and on-screen display timing. This is basically achieved by generating timing pulses in response to the horizontal synchronization pulses and signals representing time position errors of the timing pulses relative to window pulses. A **counter** generates the processed horizontal sync pulses in response to the timing pulses and is adjusted depending on whether the timing pulses are occurring inside or outside the window pulses.

BSPR:
In one preferred embodiment, a pulse detector generates a timing pulse in response to each horizontal synchronization pulse. A sync position error device generates a time position error signal for each timing pulse relative to a corresponding window pulse. A window pulse generator generates the window pulse and limits the timed position error signal to a maximum value. An acquisition device tracks when the timing pulses occur inside and outside the corresponding window pulses. An averaging device is used to generate a signal representing the average error in response to the time position errors signals. A **counter** is then used to phase-lock to the timing pulses to generate processed horizontal sync pulses. When the timing pulses occur within the corresponding windows pulses, the **counter** is adjusted by the average error signal and when a predetermined number of timing pulses occur outside the corresponding window pulses, the **counter** is loaded with a predetermined value during a timing pulse to align the timing pulses with the corresponding window

pulses.

DRPR:
FIG. 5 is a schematic block diagram of a local horizontal **counter** and window
generation circuit of the present invention;

DEPR:
The sync position error circuit 32 receives the external horizontal sync pulse
30 at a HSYNC input 34. If the external horizontal sync pulse 30 is within a
window pulse 36 received at a window input 38 (FIGS. 7-10), the rising edge
position of the external horizontal sync pulse 30 is measured relative to a
certain count in an internal **counter**, details of which will be discussed
hereinafter. This **counter** which is reset from a reset error pulse 162
generates a positive or negative time position error value if the rising edge
of the external horizontal sync pulse 30 is not centered within the window
pulse 36. This error value is output from an error output 40. If the external
horizontal sync pulse 30 is not within the window pulse 36, a 1-bit
out-of-range output 42 goes low (i.e. digital logic "0") which is applied to an
acquisition circuit 44. In addition, the time position error value is also
limited to a maximum error value because of the window pulse 36.

DEPR:
The digital output of the acquisition circuit 44 is applied to an acquire input
46 of a local horizontal **counter** 48. The local horizontal **counter** 48
essentially acts as a saw-tooth oscillator which is phase-locked to the
external horizontal sync pulse 30. The horizontal **counter** 48 is clocked by the
reference clock 22 and has a period equal to the period of a single horizontal
line in the video signal 14. That is, in NTSC format, the horizontal **counter**

48 will count from 0 to 909 and then reset to 0 and count again to 909 continuously since there are 910 samples or pixels in each horizontal scanning line.

DEPR:
When the horizontal **counter** 48 is in the "track" mode (i.e. acquire input 46=0), the horizontal **counter** continuously counts from 0 to 909 and is adjusted by an adjust input 50 after an external horizontal sync pulse 30 has occurred during a H-state update signal 52. This adjustment positions the count in the horizontal **counter** 48 so that the next external horizontal sync pulse 30 is positioned nearer the center of the window pulse 36.

DEPR:
When the horizontal **counter** 48 is in the "acquire" mode (i.e. acquire input 46=1), the horizontal **counter** 48 is loaded with a predetermined value during the external horizontal sync pulse 30. This predetermined value loads the count in the horizontal **counter** 48 into a position where the external horizontal sync pulse 30 should be positioned in the window pulse 36 during the next occurrence of the external horizontal sync pulse 30.

DEPR:
A window generator circuit 54 generates the window pulse 36 which is used to determine whether or not the local horizontal **counter** 48 is locked to the external horizontal sync pulse 30 and the relative timing or phase error of the external horizontal sync pulse 30 with respect to the window pulse 36. The window generator circuit 54 is configured to generate a window pulse 36 during which the external horizontal sync pulse 30 should occur and is preferably set to occur during counts 22 to 37 of the horizontal **counter** 48. The window generator circuit 54 also places limits on the maximum

value for the phase or
timing error.

DEPR:
The error signal from the sync position error circuit 32 is applied to an error
input 56 of a long term averaging circuit 58. The long term averaging circuit
58 receives the error value signal from the error input 56 and averages the
error value with previously accumulated error values in a leaky accumulator
which is updated once every horizontal line, details of which will be discussed
hereinafter. The signal representing the average error is then outputted at an
average output 60 which is applied to the adjust input 50 of the horizontal
counter 48. This average error signal is used during the "track" mode to fine
tune or adjust the count of the horizontal **counter** 48 such that the external
horizontal sync pulse 30 occurs substantially in the center of the window pulse
36. If the acquisition circuit 44 increments to its maximum predetermined
value, thus placing the horizontal **counter** 48 in the "acquire" mode (i.e.
acquire input 46=1), the output from the acquisition circuit 44 is also applied
to an acquire input 62 in the long term averaging circuit 58 which clears or
resets the previous accumulated average error.

DEPR:
Referring to FIG. 3, a detailed schematic block diagram of the sync position
error circuit 32 is shown. The sync position error circuit 32 includes a 4-bit
counter 122, a 4-bit digital **decoder** 124 and an AND gate 126. The 4-bit
digital **counter** 122 counts between -8 and +7 when the window pulse 36 is high
and the **counter** 122 has not counted to its maximum value of +7, as shown in
FIGS. 7-10. When the window pulse 36 is high, and the value of the **counter** 122
has not reached +7, the two inputs to the AND gate 126

are high causing the AND
gate 126 to output a digital high to a count enable input 128 of the 4-bit
digital **counter** 122. During this time, the **counter** 122 which is clocked by the
reference clock 22, outputs a 4-bit digital data stream which increments up in
binary numbers from -8 to +7 under 2's complement arithmetic which is used
throughout the digital video horizontal synchronization pulse detector and
processor 10.

DEPR:
This 4-bit digital data stream is applied to the **decoder** 124 which **decodes** the
4-bit digital data and outputs a low output when the count equals +7. When
this occurs, the output from the AND gate 126 goes low which subsequently
disables the **counter** 122 from further counting. In addition to applying the
4-bit digital data stream to the **decoder** 124, the 4-bit digital data stream is
also applied to a 4-bit latch 130. The 4-bit latch 130 latches the value of
the **counter** 122 upon receiving the external horizontal sync pulse 30 from the
horizontal sync detection circuit 24. The digital value in the latch 130
represents the error of the rising edge of the external horizontal sync pulse
30 with respect to the center of the window pulse 36, as seen in FIG. 7, when
the external horizontal sync pulse 30 occurs within the window pulse 36. If
the external horizontal sync pulse 30 does not occur within the window pulse
36, the error is limited to the maximum value of +7, to provide noise immunity
to the horizontal sync detector and processor 10. This error is outputted from
the error output 40 and received by the error input 56 of the long term
averaging circuit 58.

DEPR:
The sync position error circuit 32 also includes a 1-bit

latch 132 which
latches the window pulse 36 upon receipt of the external horizontal sync pulse
30. If the external horizontal sync pulse 30 occurs when the window pulse 36
is high, the latch 132 latches a 1-bit digital high output to the out-of-range
output 42 which indicates that the external sync pulse occurred during the
window pulse 36, as shown by the out-of-range output 42 in FIG. 7. If the
window pulse 36 is low when the external horizontal sync pulse 30 occurs, the
latch 132 latches a 1-bit digital low output at the out-of-range output 42,
shown in FIG. 9, which indicates that the external horizontal sync pulse 30 did
not occur during the window pulse 36. After each external horizontal sync
pulse 30 occurs, the 4-bit **counter** 122 and the latch 132 are reset from the
horizontal **counter** 48 with a reset error pulse 162. This reset error pulse 162
is applied to a reset input 134 of the 4-bit **counter** 122 and a reset input 136
of the latch 132.

DEPR:
Referring to FIG. 4, a detailed schematic block diagram of the acquisition
circuit 44 is shown. The acquisition circuit 44 includes an AND gate 138, a
5-bit D-Q digital **counter** 140, a 5-bit **decoder** 142 and a digital register 144.
The **counter** 140 counts up when the out-of-range output 42 is low and counts
down when the out-of-range output 42 is high. The **counter** 140 is incremented
up or down on each H-state update pulse 52, after an external horizontal sync
pulse 30 is generated. The 5-bit digital data stream from the **counter** 140 is
applied to the digital **decoder** 142 which outputs a digital high output at count
equals 0 and a digital high output at count equals 31.

DEPR:
At count equals 0, the digital high output is applied to

the AND gate 138 such
that if the out-of-range output 42 is high, indicating
the **counter** should count
down on the next H-state pulse 52, the two high inputs to
the AND gate 138
generate a high output which inhibits the **counter** 140
from counting below zero
(0). Upon reaching the count equal 31, the **decoder** 142
applies a digital high
output to the digital register 144. Upon receipt of the
next H-state update
pulse 52, the digital register 144 outputs the digital
high output to the
acquire input 46, which places the horizontal **counter** 48
in the "acquire" mode.
It should be noted that since the **counter** 140 is a 5-bit
counter, it rolls over
to a value of zero (0) after the count 31, therefore no
resetting of the
counter 140 is required.

DEPR:
Referring to FIG. 5, a detailed schematic block diagram
of the horizontal
counter 48 and the window generating circuit 54 is shown.
This circuit
includes a 10-bit digital **counter** 146 which counts up
from 0 to 909 in
increments of 1 at each reference clock pulse 22, seen in
FIGS. 8 and 10. The
counter 146 includes a load input 148, a load control
input 150 and a reset
152. When the load control input 150 receives a digital
high, the 10-bit
digital value at the load input 148 is loaded into the
counter 146 which
immediately puts the **counter** 146 at that count value.
The value at the load
input 148 is determined by a 10-bit 2-to-1 multiplexer
152 which is controlled
by the acquire input 46. The load control input 150 is
controlled by a 1-bit
2-to-1 multiplexer 156 which is also controlled or
selected by the acquire
input 46.

DEPR:

When the acquire input 46 is low, which indicates that the horizontal **counter** 48 is in the "track" mode, the value applied to the load input 148 is received from a 10-bit adder 158. The adder 158 adds the current value of the **counter** 146 with a 10-bit binary value of one (1) thereby incrementing the **counter** up by one (1). In addition, the value at the adjust input 50 which has been extended from 4-bits to 10-bits is added to the adder 158. This value represents the average error of the external horizontal sync pulse 30 with respect to the center of the window pulse 36. This loaded value from the adder 158 should substantially center the window pulse 36 with the next external horizontal sync pulse 30 so that the **counter** 146 remains locked to the external horizontal sync pulse 30. The value loaded in the load input 148 is loaded during the H-state update pulse 52 which is set to occur at count equal 50 of the **counter** 146. Thus, at count equal 50, the adder 158 adds to the count value=50, a count value of 1, plus an adjust value to position the **counter** 146 at a new value.

DEPR:
When the acquire input 46 is a digital high, indicating that the horizontal **counter** 48 is in the "acquire" mode, a predetermined fixed value of 30 is loaded, via the multiplexer 154, into the load input 148, as shown in FIG. 10. This occurs during the external horizontal sync pulse 30 which is applied to the load control 150, via the multiplexer 156, which substantially centers the window pulse 36 during the external horizontal sync pulse 30. This ultimately moves or positions the **counter** 146 into phase-lock with the external horizontal sync pulse 30.

DEPR:

The 10-bit digital data stream output from the **counter** 146 is applied to a 10-bit digital **decoder** 160 which **decodes** the 10-bit digital data stream and outputs digital high outputs at various counts. The **decoder** 160 outputs the window pulse 36 during counts 22 to 37. A reset error pulse 162 occurs at count 800 which is used to reset the 4-bit **counter** 122 and the latch 132 in the sync position error circuit 32. At count 909, a high input is applied to the reset input 152 to reset the **counter** 146 to 0 so that the **counter** continuously counts between 0 and 909. A processed H-sync 163 is generated during counts 27 to 75 which represents the regenerated digital representation of the horizontal sync pulse 16. The H-state update 52 occurs at count 50 which is used by the **counter** 146 during the "track" mode, as well as to increment the 5-bit **counter** 140 in the acquisition circuit 44.

DEPR:
Referring to FIGS. 8 and 10, the operation of the horizontal synchronization pulse detector and processor 10 is shown in a track mode and an acquisition mode as discussed above. Referring specifically to FIG. 8, the operation of the horizontal sync detector and processor 10 in the track mode is shown. FIG. 8 shows the video signal 14 and how the horizontal **counter** 48 counts with respect to the video signal 14 to produce the external horizontal sync pulse 30 within the window pulse 36. In addition, FIG. 8 shows the output of the 4-bit **counter** 122 of the sync position error circuit 32 which counts from -8 to +7 during the window pulse 36 and is reset by the reset error 162 from the horizontal **counter** 48 at count 800.

DEPR:
Referring to FIG. 10, the horizontal synchronization

CLPR:
11. The detector and processor as defined in claim 1 wherein said horizontal **counter** means includes a **counter** which is clocked by a reference clock and has a period substantially equal to the period of a single horizontal line of said video signal.

CLPR:
12. The detector and processor as defined in claim 11 wherein when the predetermined number of timing pulses occur outside said window pulse, said horizontal **counter** means is loaded with the predetermined value during said timing pulse to align said timing pulse within said window pulse.

CLPR:
19. The detector and processor as defined in claim 16 wherein said sync position error device includes an error **counter** operable to count between a predetermined error boundary during said window pulse to generate said time position error signal of said timing pulses relative to a center of said corresponding window pulses.

CLPR:
20. The detector and processor as defined in claim 16 wherein said acquisition device includes a **counter** which increments positively to said predetermined number when said timing pulses occur outside said corresponding window pulses and increments negatively to a predetermined minimum value when said timing pulses occur during said corresponding window pulses.

CLPV:
horizontal **counter** means for generating a processed horizontal sync pulse in response to said timing pulse, whereby when said timing pulse occurs within said window pulse said **counter** means is adjusted by said average error signal,

and when a predetermined number of timing pulses occur outside said window
pulse said horizontal **counter** means is loaded with a predetermined value.

CLPV:
a **counter, said counter** operable to phase lock to said timing pulses to
generate processed horizontal sync pulses, whereby when said timing pulses
occur within said corresponding window pulses said **counter** is adjusted by said
average error signal, and when said acquisition device identifies when a
predetermined number of timing pulses occur outside said corresponding window
pulses, said **counter** is loaded with a predetermined value during a timing pulse
to align said timing pulses with said corresponding window pulses.

CLPV:
adjusting a **counter** with said average error signal when the timing pulses occur
inside said corresponding window pulses;

CLPV:
loading a predetermined value into said **counter** when a predetermined number of
timing pulses occur outside said corresponding window pulses during a timing
pulse to align said timing pulses with said corresponding window pulses; and

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